WHAT WE CLAIM ARE:

1. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor substrate having current input/output regions;

(b) forming an insulating layer on the semiconductor substrate;

(c) forming a resist laminate on the insulating layer;

(d) forming an upper opening through an upper region of the resist laminate, the upper opening having a laterally broadening middle space;

(e) forming a lower opening through a lower region of the resist laminate, the lower opening communicating the upper opening, having a limited size along a current direction, and having generally vertical side walls;

(f) etching the insulating layer exposed in the lower opening;

(g) performing a heat treatment of the resist laminate to deform the side walls of the lower opening so that at least one of opposite ends of the lower region at the lower opening is retarded from a corresponding end of the insulating layer and that the lower opening has a forward taper shape upwardly and monotonically increasing a size of the lower opening along the current direction; and

(h) filling a gate electrode stem in the lower opening and forming a head in the upper opening, the head having an expanded size along the current direction.

2. The method of manufacturing a semiconductor device according to claim 1, wherein the heat treatment in said step (g) is performed at a temperature lower than a glass transition temperature of the lower region of the resist laminate.

3. The method of manufacturing a semiconductor device according to claim 1, wherein the heat treatment in said step (g) makes the opposite side walls of the lower opening along the current direction have a generally symmetric taper shape and be retarded from opposite ends of the insulating layer.

4. The method of manufacturing a semiconductor device according to claim 1, further comprising the step of (i) applying an energy beam to at least one of a pair of regions of the lower region of the resist laminate near the lower opening or a region where the lower opening is formed, wherein the heat treatment of said step (g) forms different taper shapes between a region where the energy beam is applied and a region where the energy beam is not applied.

5. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor substrate having a plurality of element regions;

(b) forming a resist laminate on the semiconductor substrate;

(c) applying an energy beam to an upper region of said resist laminate for defining an upper opening in each of said plurality of element regions, and applying an energy beam to a lower region of said resist laminate in at least part of said plurality of element regions at a dose depending on the element region;

(d) forming the upper opening through the upper region of the resist laminate in each of the plurality of element regions, the upper opening having a laterally broadened middle space;

(e) forming a lower opening through the lower region of the resist laminate in each of the element regions, the lower opening communicating the

upper opening, having a limited size along a first direction, and having generally vertical side walls;

(f) performing a heat treatment of the resist laminate to deform the side walls of the lower opening in at least some of the element regions in accordance with doses so that the lower opening has a taper shape upwardly and monotonically increasing a size of the lower opening along the first direction; and

(g) filling a conductive stem in the lower opening and forming a head in the upper opening, the head having an expanded size along the first direction.

6. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor substrate having a plurality of element regions;

(b) forming a resist laminate on the semiconductor substrate;

(c) forming an upper opening through an upper region of the resist laminate in each of the plurality of element regions, the upper opening having a laterally broadening middle space;

(d) applying an energy beam to a lower region of the resist laminate in at least some of the element regions at a dose corresponding to each element region;

(e) forming a lower opening through the lower region of the resist laminate in each of the element regions, the lower opening communicating the upper opening, having a limited size along a first direction, and having generally vertical side walls;

(f) performing a heat treatment of the resist laminate to deform the side walls of the lower opening in at least some of the element regions in

accordance with doses so that the lower opening has a taper shape upwardly and monotonically increasing a size of the lower opening along the first direction; and

(g) filling a conductive stem in the lower opening and forming a head in the upper opening, the head having an expanded size along the first direction.

7. The method of manufacturing a semiconductor device according to claim 6, wherein said step (d) applies an energy beam at different doses for different element regions, said step (f) forms the side walls of the lower openings having different taper angles, and said step (g) forms mushroom gate electrodes.

8 A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor substrate having current input/output regions;

(b) forming a first resist layer on the semiconductor substrate and baking the first resist layer at a first temperature;

(c) forming a second resist layer on the first resist layer and baking the second resist layer at a second temperature lower than the first temperature;

(d) forming an upper resist structure on the second resist layer, the upper resist structure having an upper opening having a laterally broadening middle space;

(e) forming a lower opening through the first and second resist layers, the lower opening communicating the upper opening, having a limited size along a current direction, and having generally vertical side walls;

(f) performing a heat treatment on the semiconductor substrate at a third temperature to give a relatively small forward taper to the first resist layer and

a relatively large forward taper to the second resist layer; and

(g) filling a gate electrode stem in the lower opening and forming a head in the upper opening to form a mushroom gate electrode, the head having an expanded size along the current direction.

9. The method of manufacturing a semiconductor device according to claim 8, wherein the first and second temperatures are set lower than a glass transition temperature of the first resist layer.

10. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor substrate having current input/output regions;

(b) forming a resist laminate on the semiconductor substrate, the resist laminate having a lower region and an upper region;

(c) forming an upper opening through the upper region of the resist laminate, the upper opening having a laterally broadening middle space;

(d) forming a lower opening through the lower region of the resist laminate, the lower opening communicating the upper opening, having a limited size along a current direction, and having generally vertical side walls;

(e) vapor-depositing a gate electrode insulating layer on a bottom of the lower opening from an upper side of the semiconductor substrate;

(f) performing a heat treatment on the resist laminate to deform the side walls of the lower opening so that opposite ends of the lower opening along the current direction ride opposite ends of the gate electrode insulating layer and that the lower opening has a forward taper shape upwardly and monotonically

increasing a size of the lower opening along the current direction; and

(g) vapor-depositing a metal layer into the upper and lower openings from an upper side of the semiconductor substrate to fill a gate electrode stem in the lower opening, the gate electrode stem having a bottom area inside an upper surface area of the gate electrode insulating layer, and to form a head in the upper opening to thereby form a mushroom gate electrode, the head having an expanded size along the current direction.

11. The method of manufacturing a semiconductor device according to claim 10, wherein the gate electrode insulating film is made of titanium oxide.